REMARKS

Claims 13-19 are pending in this application of which claims 13, 14, 15, 16 and 17 are independent. Claims 14-18 stand allowed. Claims 13 and 19 remain at issue.

Further to the telephone conversation with the undersigned, the Examiner refused to grant an Examiner's Interview, and requested Applicant provide comments in a response. The Examiner indicated that sufficient comment should overcome the indefiniteness rejection. Applicant's comments follow.

The Examiner has rejected claims 13 and 19 under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner posits that the amended claim language is not clear and does not read on the configuration illustrated by exemplary Fig. 6. Applicant respectfully disagrees.

Exemplary Fig. 6 illustrates a memory array 10 having a plurality of magnetic memory cells MC. Fig. 6 does not illustrate memory cells in every memory cell row and memory cell column; instead it illustrates memory cells "arranged in every other memory cell row and every other memory cell column," as claim 13 recites.

Claim 13 further recites that "that each memory cell of said plurality of memory cells is separated from another by an adjoining memory cell location in a row direction and an adjoining memory cell location in a column direction." Fig. 6 further illustrates this configuration. Each row of Fig. 6 has a corresponding Read Word Line, referred to as RWL1, RWL2, RWL3. We will refer to the rows as row 1, row 2 and row 3, respectively. Each column is bounded by a

reference voltage line SL and bit line BL. From left to right, we will refer to the columns as column 1, column 2, etc. Exemplary Fig. 6 illustrates four such columns. The notation in the upper right-hand portion of Fig. 6 illustrates the direction corresponding to "row direction" and "column direction." Therefore, in a row direction, row 1 has memory cells at columns 1 and 3. Row 2 has memory cells at column 2 and 4. Row 3 has memory cells at columns 1 and 3. In other words, in a row direction "each memory cell...[e.g. MC at row 2, column 2] is separated from another [e.g., MC at row 2, column 4] by an adjoining memory cell location [e.g., memory cell location at row 2, column 3]." Similarly, in a column direction "each memory cell MC...[e.g. MC at row 3, column 3] is separated from another [e.g., MC at row 1, column 3] by an adjoining memory cell location [e.g., memory cell location at row 2, column 3]."

Claim 19 recites that "said adjacent memory cells correspond to the nearest adjacent memory cell." As seen in Fig. 6, from the position of any memory cell, nearest adjacent memory cells are diagonal from one another. These memory cells share the corresponding line, as recited by claim 13.

The remaining figures of the application illustration variations of the configuration recited by claims 13 and 19. It is submitted that claims 13 and 19 particularly point out and claim the subject matter. Withdrawal of the indefiniteness rejection is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB/DT/dlb
Facsimile: 202.756.8087
Date: March 15, 2005

Please recognize our Customer No. 20277 as our correspondence address.